

STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR Si:C

Abstract

Structures and methods of manufacturing are disclosed of dislocation free stressed channels in bulk silicon and SOI (silicon on insulator) CMOS (complementary metal oxide semiconductor) devices by gate stress engineering with SiGe and/or Si:C. A CMOS device comprises a substrate of either bulk Si or SOI, a gate dielectric layer over the substrate, and a stacked gate structure of SiGe and/or Si:C having stresses produced at the interfaces of SSi(strained Si)/SiGe or SSi/Si:C in the stacked gate structure. The stacked gate structure has a first stressed film layer of large grain size Si or SiGe over the gate dielectric layer, a second stressed film layer of strained SiGe or strained Si:C over the first stressed film layer, and a semiconductor or conductor such as p(poly)-Si

over the second stressed film layer.